Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

BEI012 - Analog Integrated Circuit Design
Eighth Semester, 2016-17 (Even Semester)

Course (catalog) description

To have an adequate knowledge in the measurement techniques for power and energy, power and introduce the meters used to measure current & voltage.

Compulsory/Elective course : Elective for ECE students
Credit hours : 3 credits
Course Coordinator : Mrs.G.Kanagavalli, Asst. Professor, Department of ECE

Instructors :

Name of the instructor	Class handling	Office location	Office phone	Email (domain:@ bharathuniv.ac.in	Consultation
G.Kanagavalli	IV year	SA006		Kanagavalli.ece@bharathuniv.ac.in	12.30-1.30 PM

Relationship to other courses:

Pre –requisites : BEC405 Linear Integrated Circuits
Assumed knowledge : This course will teach design and analysis of analog circuits, in particular, design concepts pertinent to real world applications. It deals with the design and analysis of single stage and differential amplifiers at low and high frequencies of operation. This course introduces the design of current mirror circuits.
Following courses : Nil

Syllabus Contents

UNIT I SINGLE STAGE AMPLIFIERS 9 HOURS

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower cascade and folded cascade configurations, differential amplifiers and current mirror configurations.

UNIT II HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS 9 HOURS

Current mirrors, cascade stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascade and differential pair stages Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III FEEDBACK AND OPERATIONAL AMPLIFIERS 9 HOURS

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 9 HOURS

General considerations, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, and Other compensation techniques.

UNIT V BANDGAP REFERENCES 9 HOURS

Supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
3. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
4. Phillip E.Allen, DouglasR.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002
5. Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition

Computer usage: Nil

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area: communication | Signal Processing | **Electronics** | VLSI | Embedded

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	February 2nd week	Session 1 to 14	2 Periods
2	Cycle Test-2	March 2nd week	Session 15 to 28	2 Periods
3	Model Test	April 3rd week	Session 1 to 45	3 Hrs
5	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

To have an adequate knowledge in the measurement techniques for power and energy, power and introduce the meters used to measure current & voltage.	Correlates to program outcome		
	H	M	L
1. To describe about single stage amplifier.	d	a,b,c,e,g	J,k
2. To study about energy meters are included	a,d,e	b,c,g	J,k
3. To provide elaborate discussion about potentiometer & instrument transformers	a,d,e	b,g	j,k
4. To provide detailed study of resistance measuring methods.	a,d,e	b,g	J,k
5. To provide detailed study of inductance and capacitance measurement.	a,d,e	b,c,g	j,k
6.To study about circuit realization of the various building blocks.	a,d,e	g	j,k

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture Schedule

Session	Topics	Problem solving (Yes/No)	Text / Chapter
Unit I SINGLE STAGE AMPLIFIERS			
1.	Basic MOS physics	No	[R1]Chapter-3,4,5
2.	equivalent circuits	yes	
3.	Equivalent Models	yes	
4.	CS Configuration	No	
5.	CG Configuration	No	
6.	Source Follower cascade configuration	No	
7.	folded cascade configurations	No	
8.	differential amplifiers configuration	No	
9.	current mirror configuration	yes	
UNIT II HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS			
10.	Current mirrors, cascade stages for current mirrors	yes	[R1]Chapter-6,7
11.	current mirror loads for differential pairs	yes	
12.	Miller effect, association of poles with nodes	No	
13.	frequency response of CS	yes	
14.	CG and source follower	No	
15.	cascade and differential pair stages	No	
16.	Statistical characteristics of noise	No	
17.	noise in single stage amplifiers	No	

18.	noise in differential amplifiers.	No	
UNIT III FEEDBACK AND OPERATIONAL AMPLIFIERS			
19.	Properties and types of negative feedback circuits	No	[R1]Chapter-8,9
20.	Effect of loading in feedback networks	No	
21.	operational amplifier performance parameters	No	
22.	One-stage Op Amps	yes	
23.	Two-stage Op Amps	yes	
24.	Input range limitations	No	
25.	Gain boosting, slew rate	yes	
26.	power supply rejection	yes	
27.	noise in Op Amps	No	
UNIT IV TRANSIENT RESPONSE FOR DC CIRCUITS			
28.	General considerations	No	[R1]Chapter-10
29.	multiple systems	yes	
30.	Phase Margin	No	
31.	Frequency Compensation	No	
32,33	Compensation of two stage Op Amps	No	
34.	Slewing in two stage Op Amps	yes	
35,36	Other compensation techniques	No	
UNIT V RESONANCE AND COUPLED CIRCUITS			
37,38	Supply independent biasing	No	[R1]Chapter-11
39,40,41	temperature independent references	No	
42,43	PTAT current generation	yes	
44,45	Constant-Gm Biasing	yes	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures

- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	10%
Cycle Test – II	-	10%
Model Test	-	25%
Attendance	-	5%
Final exam	-	50%

Prepared by: G.Kanagavalli, Assistant professor , Department of ECE **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate:

(a) an ability to apply knowledge of mathematics, science, and engineering
(b) an ability to design and conduct experiments, as well as to analyze and interpret data
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability
(d) an ability to function on multidisciplinary teams
(e) an ability to identify, formulate, and solve engineering problems
(f) an understanding of professional and ethical responsibility
(g) an ability to communicate effectively
(h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context
(i) a recognition of the need for, and an ability to engage in life-long learning
(j) a knowledge of contemporary issues
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Program Educational Objectives

PEO1: PREPARATION:
To provide strong foundation in mathematical, scientific and engineering fundamentals necessary to analyze, formulate and solve engineering problems in the field of Electronics And Communication Engineering.

PEO2: CORE COMPETENCE:
To enhance the skills and experience in defining problems in Electronics And Communication Engineering design and implement, analyzing the experimental evaluations, and finally making appropriate decisions.

PEO3: PROFESSIONALISM:
To enhance their skills and embrace new Electronics And Communication Engineering Technologies through self-directed professional development and post-graduate training or education

PEO4: SKILL:
To provide training for developing soft skills such as proficiency in many languages, technical communication, verbal, logical, analytical, comprehension, team building, inter personal relationship, group discussion and leadership skill to become a better professional.

PEO5: ETHICS:
Apply the ethical and social aspects of modern communication technologies to the design, development, and usage of electronics engineering.

Course Teacher	Signature
G.Kanagavalli	

Course Coordinator	Academic Coordinator	Professor In-Charge	HOD/ECE
(G.Kanagavalli)	( )	(Dr.)	(Dr.M.Sundararajan)